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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,685	04/01/2004	Jeffrey Orion Pritchard	ALTRP117/A1404	1625

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

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06/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/816,685	**Applicant(s)** PRITCHARD ET AL.	
	Examiner Helen Rossoshek	**Art Unit** 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-23 and 25-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-23, 25-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/816,685 filed 04/01/2004 and amendment filed 03/02/2007.

2. Claims 1-3, 5-23, 25-31 remain pending in the Application.

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/02/2007 has been entered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 5-23, 25-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Sato et al. (US Patent 6,467,075).

With respect to claims 1, 30 Sato et al. teaches a method for implementing a programmable device (within semiconductor circuit synthesis method of the semiconductor circuit for executing a program with a function of pointers (col. 4, ll.56-59; col. 3, ll.8-9; ll.40-42), including a step of replacing the command which performs dynamic allocation in the code with the command which gives the pointer to the variable (col. 5, ll.17-20)), a system for implementing a programmable device (within a computer system for implementing circuit synthesis including process of pointer analysis, resolution and optimization (col. 20, ll.29-33; col. 22, ll.36-38; col. 3, ll.8-9; ll.18-21)), the method comprising:

receiving a high-level language program, the high-level language program configured to run on a conventional central processing unit (within synthesizing the semiconductor circuit of executing the program (col. 4. ll.52-53; col. 1, ll.26-27), wherein the program is C-language program (col. 5, ll.1-2) and C-language is high-level language (col. 1, ll.20-21) and wherein C-language program runs on the computer/ conventional central processing unit (col. 20, ll.28-31));

identifying a portion of the high-level language program for hardware acceleration (within partitioning the system described by high-level language "C" into software and hardware blocks to accelerate the design process of the semiconductor circuit (col. 1, ll.24-29), including the process of defining an allocation of primitives implemented in software or hardware (col. 3, 40-42; 50-53));

generating hardware acceleration logic for performing the portion of the high-level language program on the programmable device, wherein generating hardware acceleration logic comprises identifying pointer access in the portion of the high-level language program (within executing the program (C-language program) with a function of pointers and dynamic allocation (col. 4, ll.57-58; col. 3, ll.66-67; col. 4, ll.1-3)); and

coupling the hardware acceleration logic to memory (within executing the program (C-language program) with a function of pointers and dynamic allocation (col.

4, ll.57-58), wherein as a result of executing C-language program the quantity of a memory assigned in the code (col. 5, ll.11-12)).

With respect to claim 20 Sato et al. teaches a system for implementing a programmable device (within a computer system for implementing circuit synthesis including process of pointer analysis, resolution and optimization (col. 20, ll.29-33; col. 22, ll.36-38; col. 3, ll.8-9; ll.18-21)), the system comprising:

an interface operable to receive a high-level language program, the high-level language program configured to run on a conventional central processing unit (within an interface between the processes, which is defined during system partitioning (col. 12, ll.52-55; col. 3, ll.40-42) and wherein C-language program runs on the computer/conventional central processing unit (col. 20, ll.28-31));

a processor operable to identify a portion of the high-level language program for hardware acceleration and generate hardware acceleration logic for performing the portion of the high-level language program on the programmable device (within C-language program running on the computer/conventional central processing unit (col. 20, ll.28-31) for implementation of the process of defining an allocation of primitives implemented in software or hardware (col. 3, 40-42; 50-53) including partitioning the system described by high-level language "C" into software and hardware blocks to accelerate the design process of the semiconductor circuit (col. 1, ll.24-29)).

With respect to claim 31 Sato et al. teaches a method for implementing a programmable device (within semiconductor circuit synthesis method of the semiconductor circuit for executing a program with a function of pointers (col. 4, ll.56-59;

col. 3, ll.8-9; ll.18-21), including a step of replacing the command which performs dynamic allocation in the code with the command which gives the pointer to the variable (col. 5, ll.17-20)), the method comprising:

receiving a high-level language program, the high-level language program configured to run on a conventional central processing unit (within synthesizing the semiconductor circuit of executing the program (col. 4. ll.52-53; col. 1, ll.26-27), wherein the program is C-language program (col. 5, ll.1-2) and C-language is high-level language (col. 1, ll.20-21) and wherein C-language program runs on the computer/ conventional central processing unit (col. 20, ll.28-31));

identifying a portion of the high-level language program for hardware acceleration, wherein the portion is identified automatically using profiling data (within partitioning the system described by high-level language "C" into software and hardware blocks to accelerate the design process of the semiconductor circuit (col. 1, ll.24-29), including the process of defining an allocation of primitives implemented in software or hardware (col. 3, 40-42; 50-53), wherein the technique to automate the synthesis of program code with pointers and dynamic memory allocation/deallocation into hardware is implemented (col. 4, ll.42-49; col. 12, ll.1-5));

generating hardware acceleration logic for performing the portion of the high-level language program on the programmable device, wherein generating hardware acceleration logic includes pointer referencing and pointer dereferencing within executing the program (C-language program) with a function of pointers and dynamic allocation (col. 4, ll.57-58; col. 3, ll.66-67; col. 4, ll.1-3; col. 2, ll.15-17)); and connecting the hardware acceleration logic to memory (within executing the program (C-language program) with a function of pointers and dynamic allocation (col. 4, ll.57-58), wherein as a result of executing C-language program the quantity of a memory assigned in the code (col. 5, ll.11-12)).

With respect to claims 2, 3, 5-19, 21-23, 25-29 Sato et al. teaches:

Claims 2 and 22: wherein generating hardware accelerator logic includes generating HDL (col. 5, ll.1-6; col. 8, ll.57-58);

Claims 3, 5, 23, 25: wherein generating hardware acceleration logic includes generating a hardware acceleration component for implementation on the programmable device (col. 3, ll.8-9; ll.18-21)

Claims 6, 26: providing the hardware acceleration with a write port for a pointer write access identified in the portion of the high-level language program (coo. 9, ll.21-23);

Claims 7, 27: wherein the write port includes a write address line having an address corresponding to the address of the pointer (col. 9, ll.18-21; ll.61-67);

Claims 8, 28: providing the hardware acceleration with a read port for a pointer read access identified in the portion of the high-level language program (col. 9, ll.21-27);

Claims 9, 29: wherein the read port includes a read address line having an address corresponding to the address of the pointer col. 10, ll.13-16);

Claim 10: wherein the hardware acceleration component is coupled to a simultaneous multiple primary component fabric (Fig. 7);

Claim 11: wherein the central processing unit is a general purpose processor (col. 20, ll.28-31);

Claim 12: wherein the central processing unit supports a general purpose instruction set (col. 16, ll.59-65);

Claim 13: wherein the high-level language program is prepared in ANSI C (col. 18, l.49);

Claim 14: further comprising providing a processor core operable as a conventional central unit, the processor core configured for implementation on the programmable device (col. 20, ll.28-32; col. 3, ll.8-9; ll.40-42);

Claim 15: wherein the portion includes multiple disconnected sections of the high-level language program (col. 3, ll.40-42);

Claim 16: wherein the portion is identified automatically during parsing of the high-level language program (col. 2, ll.22-26; col. 4, ll.42-45);

Claim 17: wherein the portion is identified automatically using profiling data (col. 11, ll.66-67; col. 12, ll.1-5);

Claim 18: wherein the profiling data is provided by a profiling and feedback tool (col. 4, ll.42-48);

Claim 19: wherein the profiling and feedback tool identifies an optimal hardware acceleration portion (col. 4, ll.42-28; col. 9, ll.16-18);

Claim 21: wherein the processor is further configured to couple the hardware acceleration logic to memory (Fig. 7).

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Ball (US patent 7,203,799).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claims 1, 30 Ball teaches a method for implementing a programmable device (within a technique for implementing the programmable chip (col. 2, ll.39-40; col. 6, ll.61-63)), a system for implementing a programmable device (within a computer system for implementing a programmable chip (col. 11, ll.1-3; col. 6, ll.61-63)), the method comprising:

receiving a high-level language program, the high-level language program configured to run on a conventional central processing unit (within input stage 901 shown on the Fig. 9 for receiving information, such as high-level language program (col. 9, ll.1-5), wherein input stage is executed on CPU (Col. 11, ll.52-55));

identifying a portion of the high-level language program for hardware acceleration (within a generator program 905 shown on the Fig. 9 for identifying a portion of the high-level language program (col. 9, ll.29-31));

generating hardware acceleration logic for performing the portion of the high-level language program on the programmable device, wherein generating hardware acceleration logic comprises identifying pointer access in the portion of the high-level language program (within hardware accelerator 703 shown on the Fig. 7 for performing acceleration of the portion of the high-level language program (col. 9, ll.30-31) wherein generator program 905 shown on the Fig. 9 identifies pointers (col. 9, ll.33-35)); and

coupling the hardware acceleration logic to memory (within interconnections between memory component 825 and hardware accelerator 815 shown on the Fig. 8 (col. 8, ll.47-48)).

With respect to claim 20 Ball teaches a system for implementing a programmable device (within a computer system for implementing a programmable chip (col. 11, ll.1-3; col. 6, ll.61-63)), the system comprising:

an interface operable to receive a high-level language program, the high-level language program configured to run on a conventional central processing unit (within a peripheral interface 828 (col. 8, ll.42-43), wherein input stage as high-level language program is executed on CPU (Col. 11, ll.52-55));

a processor operable to identify a portion of the high-level language program for hardware acceleration and generate hardware acceleration logic for performing the portion of the high-level language program on the programmable device (within a generator program 905 shown on the Fig. 9 for identifying a portion of the high-level language program (col. 9, ll.29-31), wherein hardware accelerator 703 shown on the Fig. 7 for performing acceleration of the portion of the high-level language program (col. 9, ll.30-31) and wherein generator program 905 shown on the Fig. 9 identifies pointers (col. 9, ll.33-35)).

With respect to claim 31 Ball teaches a method for implementing a programmable device (within a technique for implementing the programmable chip (col. 2, ll.39-40; col. 6, ll.61-63)), a system for implementing a programmable device (within a computer system for implementing a programmable chip (col. 11, ll.1-3; col. 6, ll.61-63)), the method comprising:

receiving a high-level language program, the high-level language program configured to run on a conventional central processing unit (within input stage 901 shown on the Fig. 9 for receiving information, such as high-level language program (col. 9, ll.1-5), wherein input stage is executed on CPU (Col. 11, ll.52-55));

identifying a portion of the high-level language program for hardware acceleration, wherein the portion is identified automatically using profiling data (within a generator program 905 shown on the Fig. 9 for identifying a portion of the high-level language program (col. 9, ll.29-31));

generating hardware acceleration logic for performing the portion of the high-level language program on the programmable device, wherein generating hardware acceleration logic includes pointer referencing and pointer dereferencing (within hardware accelerator 703 shown on the Fig. 7 for performing acceleration of the portion of the high-level language program (col. 9, ll.30-31) wherein generator program 905 shown on the Fig. 9 identifies pointers (col. 9, ll.33-37)); and

connecting the hardware acceleration logic to memory (within interconnections between memory component 825 and hardware accelerator 815 shown on the Fig. 8 (col. 8, ll.47-48)).

With respect to claims 2, 3, 5-19, 21-23, 25-29 Ball teaches:

Claims 2 and 22: wherein generating hardware accelerator logic includes generating HDL (col. 9, ll.37-39);

Claims 3, 5, 23, 25: wherein generating hardware acceleration logic includes generating a hardware acceleration component for implementation on the programmable device (col. 2, ll.39-40; col. 6, ll.61-63);

Claims 6, 26: providing the hardware acceleration with a write port for a pointer write access identified in the portion of the high-level language program (col. 8, ll.10-12; col. 9, ll.32-34);

Claims 7, 27: wherein the write port includes a write address line having an address corresponding to the address of the pointer (col. 8, ll.10-12; col. 6, ll.15-17);

Claims 8, 28: providing the hardware acceleration with a read port for a pointer read access identified in the portion of the high-level language program (col. 8, ll.10-12; col. 9, ll.32-34);

Claims 9, 29: wherein the read port includes a read address line having an address corresponding to the address of the pointer (col. 8, ll.10-12; col. 6, ll.42-44);

Claim 10: wherein the hardware acceleration component is coupled to a simultaneous multiple primary component fabric (col. 7, ll.10-16; Fig. 7);

Claim 11: wherein the central processing unit is a general purpose processor (col. 8, ll.47-49);

Claim 12: wherein the central processing unit supports a general purpose instruction set (col. 11, ll.9-13);

Claim 14: further comprising providing a processor core operable as a conventional central unit, the processor core configured for implementation on the programmable device (col. 6, ll.64-67; Fig. 7);

Claim 15: wherein the portion includes multiple disconnected sections of the high-level language program (col. 9, ll.24-26)

Claim 16: wherein the portion is identified automatically during parsing of the high-level language program (col. 9, ll.24-26);

Claim 17: wherein the portion is identified automatically using profiling data (col. 9, ll. 24-26; ll.29-31);

Claim 18: wherein the profiling data is provided by a profiling and feedback tool (col. 9, ll.37-39);

Claim 19: wherein the profiling and feedback tool identifies an optimal hardware acceleration portion (col. 9, ll.30-31);

Claim 21: wherein the processor is further configured to couple the hardware acceleration logic to memory (col. 7, ll.4-11; Fig. 7).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ball as applied to claim 1 above, and further in view of Sato et al.

With respect to clam 13 Ball teaches the limitation from which the claim depends. However Ball lacks specifics regarding type of the high-level language program. Sato et al. teaches :

Claim 13: wherein the high-level language program is prepared in ANSI C (col. 18, l.49). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have Sato et al. to teach the specifics subject matter Ball does not teach, because it presents technique to automate the synthesis of program code with pointers and dynamic memory allocation/deallocation into hardware (col. 4, ll.43-45).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HR
05/15/2007

Helen Rossoshek
Examiner
Art Unit 2825